VERIFICATION AND SIMULATION OF NEW DESIGNED NAND FLASH MEMORY CONTROLLER

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Abstract— In this paper a NAND flash memory controller was designed. ForthebestuseofNANDtypeflashmemorywede sign a new Arithmetical and Logical Unit (ALU) for calculating increment, addition, subtraction, decrement operations etc. In this memory controller we design single memory cell, memory module, a decoder etc. These all are encapsulated inside a controller and this is on top most in hierarchy. NAND flash memory is a non volatile storage media used in today daily life electronic equipments. NAND flash memory is programmed on page by page basis. Typically programming time is very less few micro second per page. This NAND flash memory controller architecture can be used with a real secure digital card, multimedia card (SD/MMC), digital cameras etc. The NAND Flash memory controller can be an internal device, built into the application processor or host, or designs can incorporate an external, stand-alone chip. Experimental results show that the designed controller give good performance and full fill all the systemspecifications.WehaveusedFPGAchipf ordownloadour code.

Keywords-Flash memory; Non Volatile; Arithmetical and Logical Unit (ALU); Encapsulation; Field Programmable Gate Array (FPGA);Secure Digital card/Multi Media Card (SD/MMC);Hard Disk Drive (HDD);

I. INTRODUCTION

Flash memory is being widely used as a storage medium in mobile devices because of its low power consumption, small form factor, and high resistance to shock and vibration. As the density of a flash memory chip increases and the price continues to drop, the flash memory is being adopted in more diverse storage applications. Flash memory is the combination of two technologies-EPROM and EEPROM. The term “Flash” means - A large chunk of memory (memory cell) could be erased at one time”. On the other hand in EEPROM each byte is erased one by one manner.

Flash memory has characteristics that are different from conventional storage devices such as HDD. Thus, specialized hardware and software are required to use flash memory as a storage device. The role of flash memory software is particularly important because it has to deal with the peculiarities of flash memory.Italsoneedstobediversebecauseflashme moryisused inawidespectrum of applicationsrangingfrommicro-embedded systems (e.g., a sensor-node) to large-scale servers [5]. Flash memorycontrolleroffershighercapacityforfastdat atransferandrandom access of memory in I/O operations [1]. It is possible to design a simple memory mapped interface to hardware with NANDflashmemory.NANDflashmemorycontrol lerhasalsoa bidirectional bus in between peripheral devices and controller,

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controllerinternalbusforvariousfunctionalblocks andcontroller with memory connections. For the improvement of product lifetime and system performance we always design an excellent NAND flash memory controller. Single Level Cell (SLC) and Multi Level Cell (MLC) two techniques are used for storing data in memory cells. SLC offers 100,000 erase program cycle while MLC offers about 10,000 erase program cycle[2].

NAND flash memory controller has also a bidirectional bus (Data, Address, and Control). NAND flash cell are placed together for saving 60% cell size over NOR flash cells. NAND flash memory controller provides a serial access of data blocks in a very high speed [6]. Single Level Cell (SLC) and Multi Level Cell (MLC) two techniques have been used for storing data in memory cells. A software called Flash Transaction layer (FTL) use for wear leveling and bad block management technique. All vendors provide FTL software[9].

The pipelining and parallel processing concepts are applied for systematic design approach of a systolic array processor. The systolic array architecture and iterative Very Large Scale Integration (VLSI) architecture is applied for good performance. It makes the circuit design easy for implementation[8].

II.NAND FLASH MEMROY CONTROLLER ARCHITECHTURE

The capacity of NAND flash device is improved day by day, architecture are also improved day by day. Latest overall structure of NAND flash device is looks very similar to its conventional structure. A NAND flash controller implements memory mapped interface [10]. A multiplane array packs contains its own set of Cache/Data registers, more memory cells on a die and partitioned it into several plans. In multiplane array packs all operations performs parallels. Inside a single flash array operation time multiple pages of data can be programmed, read, write, fetched etc. so average data access time is small. In multiplane commands some addresses arerestricted.

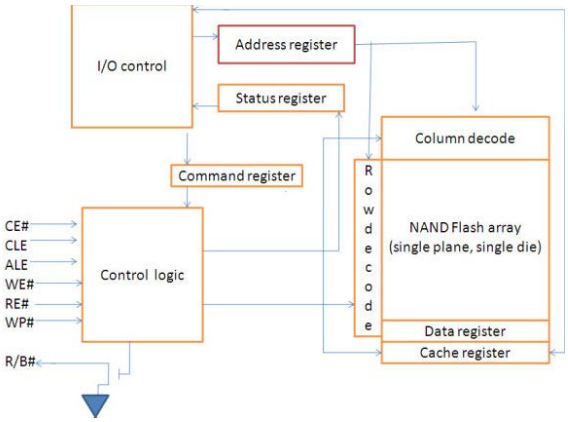

Figure 1. Block Diagram of a NAND Flash Memory Controller

NANDflashcontrollerhasflashchips.Intodaylif eitiswidely used in storage devices. One more recentapplication for flash memory is as a replacement for hard disks. Flash memory does not have the mechanical limitations and latencies of hard drives, so a Solid State Drive (SSD) is attractive when considering speed, noise,

power consumption, and reliability. It always follows

Open NAND Flash Interface (ONFI) standard [3].

In NAND flash device we have mainly I/O controlblock, control logic, NAND flash array. A NAND flash array includes two dimensional NAN D flash cells, Row/Column address decoder and cache / data registers [11]. It has a shared, multiplexed, bidirectional (command, address and data) I/O bus. Figure-1 shows the block diagram of a NAND Flash Memory Controller. A multiplane array packs contains its own s et of Cache/Data registers, more memory cells on a die partitioned into several plane. In multiplane array packs, a ll operations are performed in parallel. Thus, inside a si ngle flash array, multiple pages of data can be programm ed,read,

write, fetched, so average data access time is reduced. In

multiplane commands some addresses are restricted. So new NAND flash chip with multidie and multiplane support is always

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increase performance, reduce the data access average time, and increase parallel execution of commands

[7]. NAND flash devices are programmed on a page by page basis. Typically programming time is a fe w hundred micro secondperpage.NANDflashcellcanbeprogramm edanderased only for limited time period (100,00 0 times for SLC and 10,000 times for MLC) before it fails. To improve this limitation, flash memory performance has b een increased by using wear leveling technique. The technique spreads the memory cell use evenly to different physi cal pages. So the entire flash device is used equally to im prove the life of flash memory [2]. Bad block manageme nt technique and wear leveling technique use some remappingtechniqueoflogicaltophysicaladdresso fthememory device.TheyallprovideanFPGAtofacilitatetheim plementation ofawiderangeofNANDFlashMemoryController[4].

III. SIMULA ION ANDRESULT

A. Single Micro cellModule

In the simulation result, the NAND flash memory cell is simulated using Xilinx ISE Software and modelsim simulator. As shows in Figure 2, the RTL view of NAND Flash memory cell has been gene rated afterthe synthesis.

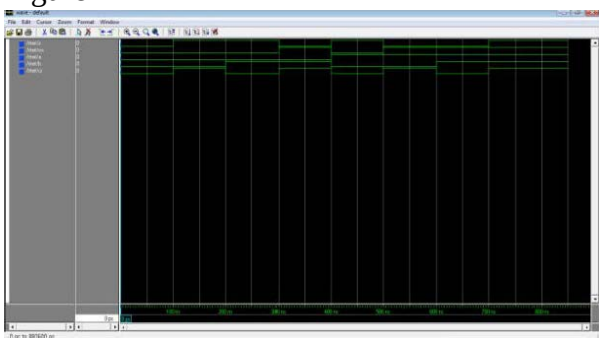
The modelsim waveform is displayed on Figure3 indicating the write and read operation. Write operation takes place only when both word line and write enable are ‘1’. The q and qbar line are modified when this situation occurs as seen in the waveform and Read operation takes place when both word line and read enable sh uld be high so that read out shows the data stored inq.

2. RTL Schematic View of Single Micro Cell Figure 3. Simulation Waveform of Single Micro Cell

B. FullAdder

The simulation of full adder carried using Xilinx ISE Software and modelsim is shown in Figure 4. The RTL view of full adder was generated after the synthesis and it displays the internal architecture of full adder. The modelsim waveforms are displaye d in Figure 5 and depict the sum and carry output. Sum tak es place only when any one input is high and carry operation is done when at least two inputs arehigh.

Figure



4. RTL Sche

Figure 5. Simulation Waveform of Ful l Addermatic View of Full Adder

C. Arithmetic and Logical Unit(ALU)

In the simulation, results of Arithmetic and Logical Unit (ALU) have been used in Xilinx ISE Software and modelsim simulator as shown in Figure 6. The RTL view of ALU has beengenerated after the synthesis and it displays the internal architecture of ALU. The mod elsim waveform is displayed in Figure 7 which indicates all mathematical operations. The additionoperationtakesplaceonlywhenop_sel.Op erationselect lines are zero a nd provide input value to the dat_a and dat_band chec k the results on dat_out as well as all flag register like carry flag, Sign flag, auxiliary carry flag, parity flag, etc. Thus all mathematical operation can be carried by changing the value of op_sel.

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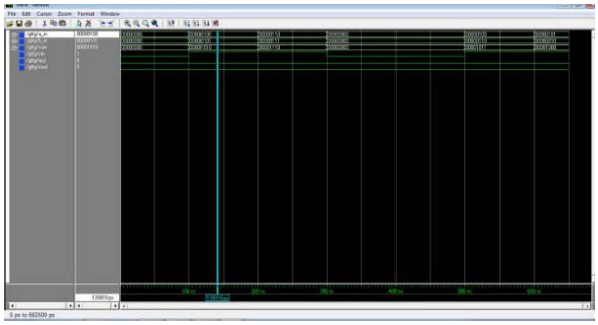


D. Memory Module

In the simulation, result of Me mory Unit using Xilinx ISE Software and modelsim simulator are shown in Figure

8. The RTL view of memory unit is generated after the synthesis to display the internal architecture of Memory Unit. The modelsim waveform is displayed in Figure 9. It indicates how the data can store in to the memory with the help of read and writeoperation.

E. Memory ReadCycle

In Figure 10, the RTL view of Memory Read Cycle has been generated after the synthesis to display the internal architecture of Memory Read Cycle. The modelsim waveform is displayed in Figure 1 1. During Memory Read Cycle when reset = '1' then both the mode operationare

zero and when apply the clock pulse the data at ¼ and ¾ points in data cell is generated and when increment the clock the data are in a position to g o from serial to parallel conversion. After some time it will also shift to data register. In this way, data are shifted tothe particular data register and finally read the data at thatlocation.

F.Memory WriteCycle

InFigure12,theRTLviewofMemoryWriteCycl ehasbeen generated after the synthesis to display the internal architecture ofMemoryWriteCycle.Themodelsimwaveformis displayedin Figure 13. During Memory Write Cycle when reset = '1' then

both the wrn1 and wrn2 operation is one and when enable the clock detect the edge on write pulse. After some time, detect edge on write pulse to load transmit buffer. When increment the clock the data are in a position to go from transmit shift register to transmit buffer. In this way, data are shifted to the particular data register and finally write the data at that location.

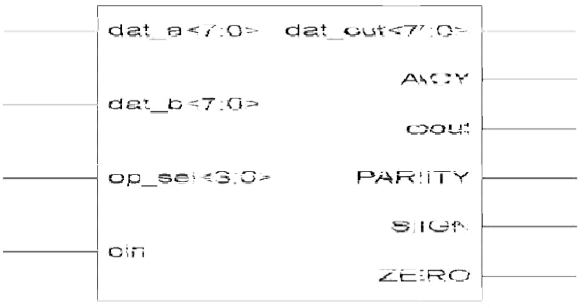
G. NAND Flash Memory Controller

Figure 14 shows Xilinx RTL Schematic view of NAND Flash Memory Controller. Figure 15 are shows the Simulation Waveform of NAND Flash Memory Controller. We bind all the above components inside this module. This module is stand at the top of hierarchy. Various pins are describedbelow-:

- nand_ale :This

pin indicates NAND flash advanced latch enable when this pin is high, the NAND flash memory controller work and when it is low, the NAND flash memory controller are in latch mode.

- nand_ce : This pin indicates NAND flash chip enable. When this pin is high the NANDflash memory controller are in working mode, it reflects that the data is storing in a memory in sequential order. When it is low, the NAND Flash memory controller do notworked.
- nand_cle: This pin indicates NAND flash clear mode. When this pin is high the data are cleared in the main memory of NAND flash memory controller. When it is low it will notworked.
- nand_re: This pin indicates NAND flash reset. When this pin is high the NAND flash memory controller are in reset mode i.e. all operations of NAND flash memory controller stopped. When it is low, it will workproperly.



- nand_tri_en: This pin indicates NAND flash tri- state enable. When it is high, it will indicate the data are in tri-state i.e. high impedance state. When it is low it may workproperly.
- nand_we : This pin indicates NAND flash

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in write operation. When it is high, data are in writing process in a write mode i.e. we can write the data at particular memory address. When it is low, it will not provide a permission to write the data.

- nand_opr<2:0> : This pin indicates selection between reset state (000), read IDstate (001),read page state (010) and write page state (011). After that state 100,101,110,111 (4 states) reserve for future extension.
- nand_rdy : This is the NAND flash ready input signal from the memory device, only accessible when high. If it is low it will not beaccessible.
- prog_2,prog_3,…prog_24 :These 23 pins used for writestates
- read_2,read_3,…read_21 : These 20 pins used for readstates.
- rid_2, rid_3, ….,rid_9 : These 8 pins used for select IDstates.
- rst_low:This pin indicates the reset input of the system. It is normallylow.
- rst_1, rst_2, rst_3 : These 3 pins used for reset states.

CONCLUSION

In this paper NAND flash memory controller for SD/MMC memory card using FPGA was designed. The test results show that NAND flash memory controller architecture will achieve a high performance. In the proposed NAND flash memory controller, all the blocks like microcell, microcontroller, ALU, fulladder,memoryunit,memoryreadcycle,memorywritecycle havebeendeveloped.Proposedarchitecturecanworkwithallthe embedded computing system as a replacement of conventional Hard Disk Drive (HDD) with a very huge size of NAND flash memory. In this controller we design only four states reset state, read ID state, read page state, write page state. In future extension we have four reservestates.

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Figure 15. Simulation Waveform of NAND Flash Memory Controller International Conference on Control and Automation, Page 609- 614, 2009.